Remarks

As related to the examiner in voice mail messages, including on July 19, 2007, commensurate with the examiner's remarks in the office action letter of June 22, 2007 (which was reissued on July 25, 2007), applicants hereby amend the application to place the claims in allowable condition. Thus, the present claims amendments and new claims are submitted herewith, and claims 6, 8, 10, 17 and 19 have been cancelled. However, by the present amendments and claim cancellations, applicants are not conceding in this application that claims 1-19 as originally submitted are not patentable over the prior art of record. The present amendments and cancellations are made only for facilitating expeditious prosecution of other subject matter believed allowable, and applicants respectfully reserve the right to pursue the originally submitted claims 1-19 in one or more continuation and/or divisional patent applications.

Claim Rejections 35 USC § 101

Claims 1-11 and 19 stand rejected under 35 USC § 101 as directed to non-statutory subject matter. Claim 1 has been amended to claim a method for ordered command verification testing of a multiprocessor computer system comprising multiple parallel processor threads, comprising a semaphore manager sequentially distributing a composite test sequence of commands as defined in the body of the claim to a plurality of the processor threads and observing the performance of the threads in response to the distributed test commands. Thus, amended claim 1 is now believed to produce a tangible, useful and concrete real-world result and to be, therefore, allowable under 35

USC § 101. Claims 2-5, 8 and 10 are dependent upon amended claim 1 and accordingly incorporate all of its limitations. They are also, therefore, believed allowable under 35 USC § 101 for the same reason.

Claim 19 has been cancelled. New claim 20 claims an article of manufacture comprising a computer readable medium having a computer readable microprocessor semaphore manager program embodied in said medium, wherein the semaphore manager program, when executed on a computer, causes the computer to distribute test commands to multiprocessor computer system processor threads and observe the performance of each of the of threads in response to the distributed test commands. Thus, new claim 20 is now believed to produce a tangible, useful and concrete real-world result and to be, therefore, allowable under 35 USC § 101. New claims 21-25 are dependent upon new claim 20 and accordingly incorporate all of its limitations. They are also, therefore, believed allowable under 35 USC § 101 for the same reason.

Claim Rejections 35 USC § 102

Claims 1-2, 9-13 and 16-19 stand rejected under 35 USC § 102(e) as being anticipated by Parson (U.S. Pat. No. 6950963). Prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. Jamesbury Corp. v. Litton Indus. Products, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); Atlas Powder Co. v. du Pont, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); American Hospital Supply v. Travenol Labs, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984).

Claim 1 has been amended to claim a method for *ordered semaphore command verification testing* of a multiprocessor computer system comprising multiple parallel

processor threads, comprising forming a plurality of buckets of *legally ordered sequences* of *semaphore* test commands, and *randomly* selecting, ordering and combining the buckets in sequential bucket test combinations wherein an order of any of the buckets relative to another of the buckets within the test sequential order may be *changed* within the test sequential order, and the test sequential order remain *legal* and thereby generating a *predictable result* when executed by the threads. Moreover, a *semaphore* manager sequentially distributes the composite test sequence commands to a plurality of the processor threads and observes their performance.

As established in the specification, the claimed method provides a significant advantage not taught or discussed by Parson wherein discrete groupings or "buckets" of legal *ordered semaphore* command sequences may be combined and run together, wherein each bucket will run individually without violating any semaphore filter rule and, most importantly, a number of buckets may be strung together and run in a large compound series without violating the filter rules. "Legal" combination of commands refers to a sequence of commands that should produce predictable results, in contrast to illegal or undesirable command sequences that result in a system hang or unpredictable result, even when a computer system design is implemented correctly. Legal combinations may also include error scenarios in which the logic should predictably recover. True randomness may now be introduced in the selection of buckets, the order of buckets selected and strung together, and in the thread selected and tested by the manager. See the published specification at paragraphs 0014 and 0018.

In contrast, Parson teaches a control mechanism that dynamically defines a group of processors subject to common control, receives one or more commands for each of

the processors in the group, and *delays issuance* of at least a subset of the commands for the group until a *designated group scan command* is received for each of the processors in the group. See Parson, column 2, lines 55-63. Parson offers <u>no</u> recognition of the problem, or teaching to one skilled in the art on groupings or "buckets" of <u>legal ordered semaphore commands sequences</u> which may be combined and run together in a large compound series <u>without</u> violating any semaphore rule and thereby configured to produce predictable results, in contrast to illegal or undesirable command sequences that will result in a system hang, unpredictable results or wherein the logic will <u>not</u> recover. Thus, amended claim 1 is believed to be allowable under 35 USC § 102 in view of Parson.

Independent claims 12 and 20 claim a verification system and article of manufacture, respectively, incorporating limitations corresponding to those of amended method claim 1 discussed above, and are thus also believed allowable under 35 USC § 102 over Parson for the same reasons. Claims 2, 9, 11, 13, 16, 18 and 21-25 are all directly or indirectly dependent upon claims 1, 12 or 20 and, therefore, incorporate all of their respective limitations, and are also believed allowable under 35 USC § 102 over Parson for the same reasons.

Amended dependent claims 9 and 16 and new dependent claim 24 also claim limitations wherein a value assigned to a parameter within an executable command causes a responsive identification and selection of a next thread for a next command distribution. This provides specific advantages in the verification environment by providing flexibility in that, whenever a verification command is needed, it is provided through use of the same parameters. All operation and verification model commands

look the same to the multiprocessor system, and the verification models use the operations code parameters to figure out a destination for each command. See the applicants' published specification at paragraphs 0020-0021. These specific claim limitations are not taught or disclosed by Parson, and claims 9, 16 and 24 are, therefore, believed allowable under 35 USC § 102 over Parson for these additional reasons.

Amended dependent claims 11 and 18 and new dependent claim 25 also claim limitations wherein a semaphore is randomly selected and unlocked in response to the parameter value. This provides specific advantages by providing that within each bucket the parameters of each instruction may be fixed or they may be randomized; for example, a central manager may randomly pick a semaphore to be unlocked by the command. See the applicants' published specification at paragraph 0025. These specific claim limitations are not taught or disclosed by Parson, and claims 11, 18 and 25 are, therefore, believed allowable under 35 USC § 102 over Parson for these additional reasons.

Claim Rejections 35 USC § 103

Claims 3-8 and 14, 15 stand rejected under 35 USC § 103(a) as being unpatentable over Parson in view of Duggan (U.S. Pat. No. 6,002,871). Claims 3-8, 14, 15 and 22-25 are all directly or indirectly dependent upon claims 2, 13 or 21, incorporate all of their respective limitations, and are thus believed allowable under 35 USC § 103 over Parson for the reasons discussed above with respect to the 35 USC § 102 rejections of claims 1-2, 12-13 and 20-21.

Moreover, 35 USC § 103(a) forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject

matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. <u>Ex parte Catan,</u> __ Westlaw __ (PTO Bd. App. & Int. July 3, 2007), citing <u>KSR Int'l Co. v. Teleflex Inc.</u>, 127 S.Ct. 1727, 1734, 82 USPQ2d 1385, 1391 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art. *Ibid.*, citing <u>Graham v. John Deere Co.</u>, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966).

Amended dependent claims 3 and 14 and new dependent claim 21 claim limitations wherein the composite test command sequence further includes a wait command, and wherein a semaphore manager is configured to pause for at least one instruction cycle, skip a next thread and distribute a next command ordered subsequent to the wait command to an <u>alternative thread</u>, the manager thereby sequentially tests each of a <u>different second plurality</u> of the processor threads. This provides specific advantages by enabling the efficient testing of *corner cases* by providing a means (cycles of wait/downtime) during a testing sequence that manipulates the selection of threads selected by a semaphore manager and forces a different (second) plurality of threads to run the ordered test sequence, wherein the second plurality but not the first will evidence error behavior when executing the same ordered commands. See the applicants' published specification at paragraphs 0033-0035.

These specific claim limitations are not taught nor disclosed by Parson, and Duggan does not provide the missing teachings, nor any cognizance of the problem of corner cases or how to find them through wait commands incorporated into order semaphore

testing operations, nor would the use of wait commands as claimed be obvious to one skilled in the art at the time the invention was made in view of Parson or Parson in view of Duggan. Although Duggan discusses a wait command, Duggan's wait command causes his computer "to pause *five seconds*, simulating, for example, the time it takes a real user to read a logon screen of the application program under test." See Duggan at column 12, lines 30-45. And also "[t]he WAIT command is used in a test script to *simulate the time it takes a real user to, for example, read a web page of a web application under test...* Concurrency depends on these *simulated wait periods*, as it is during a wait period of one session that another session can gain control (through reentrancy) of the test tool program to execute a command of that session." See Duggan at column 23, lines 1-12.

Thus, Duggan teaches application-specific testing for application performance level impact by simultaneous multiple user request by using wait commands on a vastly different timing scale, wait commands which <u>cannot</u> achieve the corner case testing achieved by applicant's claimed invention. It would <u>not</u> have been obvious at the time the invention was made to a person having ordinary skill in the art to target an individual processor thread for testing, nor would one understand or be cognizance of the importance of testing different individual processor *threads* within a *multiprocessor* for errors in command execution, or how to do so with the same command groups through use of waits commands. Claims 3, 14 and 21 are, therefore, believed allowable under 35 USC § 103 over Parson in view of Duggan for these additional reasons.

Claims 4-5, 7, 10, 15, 16, 18 and 23-25 are all directly or indirectly dependent upon claims 3, 14 or 22, incorporate all of their respective limitations, and are thus believed allowable under 35 USC § 103 over Parson for the reasons discussed above with respect

to the rejections of claims 1-3, 12-14 and 20-21. Moreover, Parson in view of Duggan does not teach the random wait command insertion and parameter value setting techniques specifically claimed by one or more of said claims 4-5, 7, 10, 15, 16, 18 and 23-25, and they are each also believed allowable over Parson in view of Duggan under 35 USC § 103 for these additional reasons.
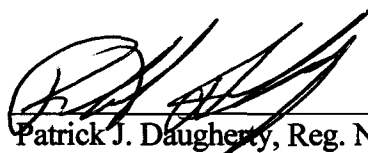
Conclusion

Claims 1-5, 7, 9, 11-16, 18 and 20-25 are now believed in condition for allowance, and early issuance of the appropriate notification of allowance is respectfully requested.

Respectfully submitted,

Date: _____

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